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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,743	03/23/2004	John Joseph Ellis-Monaghan	BUR920020074US2	2742

23389 7590 09/07/2004

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EXAMINER	
ABRAHAM, FETSUM	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,743	ELLIS-MONAGHAN ET AL.	
	Examiner	Art Unit	
	Fetsum Abraham	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *the rest* is/are rejected.

7)☒ Claim(s) *13,25 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the BICMOS element in the claims must be shown or the feature(s) canceled from the claim(s). The submitted drawings only shows bipolar and MOS transistors, which are structurally different from known BICMOS devices.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **1-12,14-24,26-28** is rejected under 35 U.S.C. 103(a) as being unpatentable over Inoh et al (5,620,908).

The patent discloses an SOI based bipolar transistor in figure 2A composed of SOI structure having a bottom silicon containing layer (100), a buried insulation layer (108) on the silicon containing layer, a sub-collector (101) on the top surface of the bottom silicon containing layer, the sub-collector in direct contact with the bottom surface of the bottom insulation layer, a top silicon layer (110) on the insulation layer, selectively etching the top silicon layer (110), the buried insulation layer ((108) and stopping t the atop the sub-collector layer (110) to define an area for forming a bipolar transistor, and forming a base area (109) in the etched area directly on the sub-collector (101).

Although the structure omits to extend the product such that it also alternatively apply for heterojunction transistors, material choice has been notoriously known in semiconductor art for one skilled in the art to find obvious exchanging the semiconducting materials with heterojunction materials according to specific anticipated result/application, since the choice of material depends on speed, conduction, resistance, and optical or electrical applications.

As for claims 2,12,21 ion implantation is an alternate means of forming layers to thermal diffusion that is notoriously known in the art since it provides deep penetration of ions into a semiconducting material in much faster time for one skilled in the art to utilize the method to save processing time. As for the effect of ion implantation in altering the conductivity of a given layer, all implantation processes are performed to achieve the same.

As for claim 3, the sub-collector is formed during the formation of the overall SOI structure.

As for claims 4,22, the collector contact region (121) is formed in the SOI structure.

As for claims 5,6, trench isolation a known technique of isolating device to protect the same from cross talk induced problems. Further, deep or shallow trench isolations are normally formed either ahead or after the formation of devices. Specifically, deep trench isolations are used in high integration environment, while shallow trench isolations are used in circumstances where high integration is not required. The technology, however, is old and has been commercially available for a long time for one skilled in the art to utilize for the reasons above.

As for claim 7, the top silicon material (115) is removed prior to the etching process of the insulator under. Clearly, the etchant materials also differ for the two types of materials.

As for claims 8,10, the base material is an epitaxial layer while said "low temperature" processing conditions are relative and subjective choice. The self aligned

and non-self aligned base structure in claim 10 translates to the two most common processes known in the art and the base structure of the prior art is self-aligned.

As for claims 9,17,18 layer (109) is a silicon base region and layer (115) is a doped polysilicon base region. Clearly, the classification of a silicon layer includes monocrystalline

As for claim 11, a patterned isolation oxide is formed atop the base region on both sides of the emitter (122).

As for claim 14, similar to the claimed devices based on the drawings, there is a MOS transistor in figure 2A of the prior art. Please note that the examiner treats the BICMOS as a MOS device based on the submitted drawings that omits to show a BICMOS.

As for claim 15, the field effect device is adjacent to bipolar transistor.

As for claim 16, a MOS capacitor, a passive element associated with the second transistor is on the substrate. Furthermore, the existence of passive/active elements on the same substrate does not carry allowable subject matter so long as the elements are independent of each other, since it is a common practice in the art to form such devices on the same substrate to simplify processing steps and achieve better circuit density.

As for claim 20, the method of making the structure includes a bipolar dielectric material (113) within the base region.

As for claims 23,24 there is a liner insulation material on the sidewalls of the upper portion of the trench where the bipolar transistor is formed directly on the bipolar dielectric material.

As for claim 27, one of the two P-type and N-type materials are used to make bipolar transistors depending on the type of transistor and the technology of the prior art is favorable for both types of transistors.

As for claim 28, ion implantation one of the known methods of increasing layer conductance. Therefore, it would have been obvious to one skilled in the art to use the method instead of thermal diffusion to achieve the same result in a shorter processing time.

Claims 13,25,29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham whose telephone number is: 571-272-1911. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915.

Fetsum Abraham
9/1/04